REMARKS

In response to the Office Action mailed on 15th December, 2004, Applicant wishes to enter the following remarks for the Examiner's consideration. Applicant has amended claim 1 and 9-13. Claims 1-13 are pending in the application.

Claim Objections

Claims 1 and 11-13 have been objected to because of informalities. Claims 1 and 11-13 have been amended as suggested by the examiner to overcome these informalities. However, the Applicant submits that the "execution time" of a test is an inherent property of the test and hence the use of "the execution time" rather than "an execution time" is proper.

Rejection of claims under 35 USC §112

Claim 9 has been rejected 35 USC §112 for lacking antecedent basis for "the optimized set". Claim 9 has been amended to depend from claim 2 which provides proper antecedent basis for this limitation.

Rejection of claims under 35 USC §101

Claims 1-13 has been rejected 35 USC §101 as being directed towards non-statutory subject matter. Applicant respectfully traverses this rejection of the claims.

Claim 1 is directed towards a process for eliminating redundant tests and the reordering of one or more inefficient tests in digital integrated circuits (IC's). The elimination and reordering of IC test is clearly useful in reducing the duration of post-production testing of integrated circuit (page 2, lines 23-

29) and in reducing the number of tests required to detect defective devices (page 3, lines 21-28).

Claim 1 has been amended to clarify how the claimed method is useful for selecting an optimal test sequence from a sequence of N tests for detecting faults in digital integrated circuits (IC's). In particular, the elements "selecting a first test in the optimal test sequence to be the test represented by the first correlation vector" and "selecting a next test in the optimal test sequence to be the test represented by the next correlation vector" have been added to clarify how the selection of correlation vectors relates to the selection of the test sequence.

Claims 11-13 have been amended similarly.

Rejection of claims under 35 USC §103(a)

Claims 1-13 have been rejected under 35 USC §103(a) as being obvious in light of Saw et al. (Patent No. US 5,345,450). Applicant respectfully traverses this rejection of the claims.

Firstly, as the examiner points out, the method of Saw et al. is directed towards reducing the simulation time of a series of tests for a logic device (col. 2, line 65 to col. 3, line2). In contrast however, claims 1-13 are directed towards reducing the number of tests applied to an actual digital integrated circuit (IC) or the total testing time of the IC (page 3, lines 21-28). Claims 1-13 refer only to digital integrated circuits (ICs) and make no reference to simulations of logic devices. Saw et al. col. 5. lines 4-27 describe how their 'redundant' tests do not affect the execution time of the actual test, but only affect the simulation time. This teaches away from using their method to reduce execution time.

Secondly, Saw et al. col. 2, lines 46-63 describe that the test are 'redundant' because the same test is repeated multiple times. Clearly, a

simulation will give the same result every time if the input is unchanged, so repeating a test is waste of time. In contrast, in the present invention, a test is redundant if it gives no information that is different from a set of previous (but different) tests. I.e. in Saw et al. a test vector is redundant if it is a duplicate of another test vector – regardless of what device it is applied to, whereas in claims 1-13 a test is redundant if it provides no extra information about faults on a particular set of L devices.

Thirdly, in claims 1-13, each test is represented by a correlation vector. As defined in the specification on page 4, lines 2-7, "Each of the N vectors has L components, corresponding to the L DD's. For each of the N tests, we create a correlation vector, V. For test i, we have

$V(i) = (v_1(i), v_2(i),\ldots, v_L(i))$,

where $v_j(i)$ is equal to zero if test i does not detect DD j and is equal to one if test i detects DD j. "

Thus there is a correlation vector associated with each test, but the correlation does not specify what that test was. The length of the correlation vector is equal to the number of defective dice tested. Claims 1 and 11-13 have been amended to make this definition of a correlation vector explicit.

In contrast, Saw et al., figure 8b, shows test vectors, not correlation vectors. In the Saw reference, each test vector (each row of the table) is a vector of input signals (logical values) that are applied at a specific time to the inputs of a chip. Thus, each row of the table represents a signal vector for a test, and the elements of the row represent the signals applied during the test. The length of the test vector is equal to the number of inputs on the device to be simulated. Thus, an element of a correlation vectors denote the result of applying a test to particular device, whereas an element of test vector represents the actual signal applied to an specific input during a test. This is

not merely a difference in terminology, the test vectors of Saw et al. and the correlation vectors of the present invention have completely different meaning.

The methods in claims 1-13 include the elements of finding and updating a vector W. For example, in claim 1, the elements of the vector W indicate whether any of the tests selected have identified a fault in the corresponding defective die. Saw et al. consider only the inputs to a device under test, they do not consider the results of the tests. Applicant must take exception with the characterization by the Examiner that the discovery and update of the vector W is merely a 'terminology'. Rather, these are specific elements of the claimed method and no equivalents in the Saw et al. reference have been cited by the examiner.

The methods in claims 1-13 include the element of calculating the products of correlation vectors with the vector W. This element is not taught by Saw et al. Since Saw et al. identify only duplicated test vectors, the vectors can be compared element by element. Further, to identify duplicate test vectors, a test vector is compared with the preceding test vector, not with a W vector. Still further, Saw et al. consider only test vectors, not correlation vectors.

In light of the foregoing amendment and remarks, Applicant respectfully submits that the Saw et al. reference does not teach, suggest, disclose or otherwise anticipate the recitations of the claims. Further, the Saw et al. reference is directed towards a different problem (simulation of tests rather than actual test) and teaches that their method cannot be used to address the problem addressed by the present invention. Accordingly, there is no

motivation to modify the approach of Saw et al. to obtain a method for reducing execution time of a test.

Still further, the Saw et al. reference does teach, suggest, disclose or otherwise anticipate the use of correlation vectors. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

In light of the foregoing amendments and explanations, applicant submits that all rejections of claims 1-13 have been overcome. The scope of the amended claims is substantially the same with implicit meaning now made explicit. Allowance of claims 1-13 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

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